Novel Duty Phase Control for Single-Phase Boost-Type SMR

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***Abstract*- In this paper, a novel duty phase control (DPC) for single-phase boost-type switching-mode-rectifier (SMR) is developed and implemented in DSP-based system. Compared to the conventional multi-loop control structure with inner current loop and outer voltage loop, noted that there is only one voltage loop tuning the phase of pre-defined duty pattern (i.e. duty phase) in the proposed DPC. Due to no current loop, inductor current sampling and tracking control are unnecessary when SMRs are operated to obtain sinusoidal current waveform and regulate the output voltage. It implies that the single-loop DPC is simple, current sensorless and loopless, and is very adaptable to the implementation with digital and analog integrated circuits. In this paper, first, the effect of the duty phase on the input current is analyzed and modeled. It shows that the sinusoidal current waveform can be naturally generated by the pre-defined duty pattern and the current amplitude is roughly proportional to the controllable duty phase. Then, a voltage controller is designed to regulate the dc output voltage by tuning this duty phase. Finally, some simulated and experimental results have been given to illustrate the performances of the proposed DPC.**

I. INTRODUCTION

The AC/DC converter is an essential component for most power electronic systems to build up DC-link voltage source from the AC mains. The use of switching-mode-rectifier (SMR) [1-3] with power factor correction (PFC) function is an effective mean to perform the AC/DC conversion with high quality by shaping the input current waveform and regulating the output voltage. The boost-type SMRs are the most popular circuit topology among all the others to shape the current waveform for their continuous current in the front-end inductors [1].

In order to let the boost-type SMRs have good input and output performances, many types of voltage and current control approaches have been developed, such as feedforward current control [3-5], robust voltage and current control [3,6] and predictive current control [7-8]. The multi-loop control is the most popular structure to coordinate the individual voltage and current control to meet the input and output specifications by controlling the single power switch.

However, there are two drawbacks in the common multi-loop control for boost-type SMRs. One is that the output voltage ripple through the outer voltage loop will result in the distorted current command into the inner current loop. The other is the difficulty of deciding the current sampling instants due to the large variations in the switching duty of the boost-type SMRs. However, it is cleared that the above two problems are relating to the inner current loop and, thus, if there is no current loop in the control structure, both the problems and the cost of current sensing can be removed in the operations of boost-type SMRs. It implies that only one voltage loop is included in the final control structure, and thus, such single-loop control structure is very competitive for its simplicity.

The proposed duty phase control (DPC) can be seen as the single-loop structure with only one voltage loop tuning the phase of the pre-defined duty pattern (i.e. duty phase). Compared to the simple single-loop voltage mode control under discontinuous current mode (DCM), the proposed single-loop DPC is working in continuous current mode (CCM). Therefore, the developed DPC is novel, easy, current sensorless and loopless.

The paper is organized as follows. Initially, the phase effect of the pre-defined duty pattern on input current is analyzed and modeled. The results show that the sinusoidal current waveform can be automatically generated by the pre-defined duty pattern and the input current amplitude is roughly proportional to the duty phase. Subsequently, based on the effect of duty phase on the input current amplitude, a voltage controller can be included to regulate the dc output voltage by means of tuning the duty phase. Finally, some simulated and experimental results have been given to illustrate the performance of the proposed DPC. The measurements also show that the drawn harmonic currents are well below the limits of the standard IEC 61000-2-3.

II. BOOST-TYPE SMRS

A. Modeling

As shown in Fig. 1, the power circuit of the boost-type SMR mainly consists of a diode bridge rectifier and a boost-type DC/DC converter. In order to model the behaviors of the boost-type SMR, some assumptions are initially made:

(i) Circuit elements are ideal and thus, lossless;
(ii) Power switch *SW* operates at a switching frequency approaching infinity.
(iii) A bulk capacitor C_d is included in the power circuit and the output voltage v_d can be assumed to be the average value V_d.

Therefore, the above three assumptions allows the following equation on an instantaneous basis.

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$$P_s(t) = P_d(t) = v_d(t) i_d(t) \approx V_d i_d(t) \tag{1}$$

where $P_s(t)$ and $P_d(t)$ are the instantaneous input power and output power, respectively. Furthermore, when the boost-type SMR is operating in CCM with unity power factor, the drawn input power $P_s(t)$ can be expressed as the product of input current $i_s(t) = \hat{I}_s \sin(\omega t)$ and input voltage $v_s(t) = \hat{V}_s \sin(\omega t)$.

$$\begin{aligned} P_s(t) &= v_s(t) i_s(t) = \hat{V}_s \sin(\omega t) \times \hat{I}_s \sin(\omega t) \\ &= \frac{\hat{V}_s \hat{I}_s}{2} - \frac{\hat{V}_s \hat{I}_s}{2} \cos(2\omega t) \end{aligned} \tag{2}$$

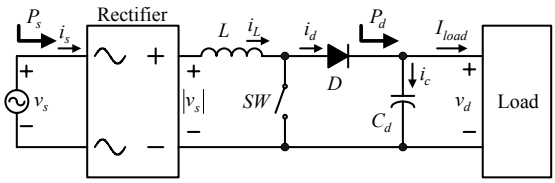

Fig. 1. Power circuit of the boost-type SMR.

Therefore, from the above two equations, we can obtain output current

$$i_d(t) = \frac{P_s(t)}{V_d} = \frac{\hat{V}_s \hat{I}_s}{2V_d} - \frac{\hat{V}_s \hat{I}_s}{2V_d} \cos(2\omega t) \triangleq I_{load} + i_c(t) \tag{3}$$

where the average value of i_d is

$$I_d = I_{load} = \frac{\hat{V}_s \hat{I}_s}{2V_d} \tag{4}$$

and the current through the capacitor is

$$i_c(t) = -\frac{\hat{V}_s \hat{I}_s}{2V_d} \cos(2\omega t) = -I_d \cos(2\omega t) \tag{5}$$

Then, the ripple $v_{d,ac}$ in v_d can be estimated from (5) as

$$v_{d,ac}(t) \approx \frac{1}{C_d} \int i_c(t) = -\frac{\hat{V}_s \hat{I}_s}{4\omega C_d V_d} \sin(2\omega t) \tag{6}$$

B. Multi-Loop Control

The above derivations (1)~(6) are mainly from considering the relations between input and output waveforms and neglecting the detailed switching behavior of the boost-type SMRs. Therefore, as shown in Fig. 2, the popular multi-loop control for boost-type SMRs are not based on (1) through (6) but based on the following straightforward principles of waveform tracking and power balance.

From the balance between input and output power, the adequate input current amplitude can be certainly obtained to maintain the desired output voltage. Therefore, in the multi-loop control shown in Fig. 2, the input current amplitude $\hat{I}^*$ can be yielded to regulate the output voltage through the outer voltage controller. By multiplying $\hat{I}^*$ with the unity rectified signal $s(\omega t) = |\sin \omega t|$, the inductor current command i_L^* of desired load condition can be obtained. In order to shape the current waveform, the switching signal $d(t)$ in Fig. 2 is generated by comparing the output signal v_{cont} of the current controller in (+) input and an unity triangular signal v_{tri} possessing frequency f_{tri} in (-) input.

However, we can find two drawbacks in the above multi-loop control. The first one is that some significant ripple voltage on the DC bus voltage $v_d(t)$ will result in the existence of double line-frequency component in the current command magnitude $\hat{I}^*$ by the voltage controller. Then, it follows that the line current waveform is regulated to follow a distorted current command waveform. The second drawback is the difficult decision to determine the current sampling instants due to the large variation of the switching instants in the boost-type SMRs. However, the above two problems are relating to current control loop and both can be removed by developing current loopless controller.

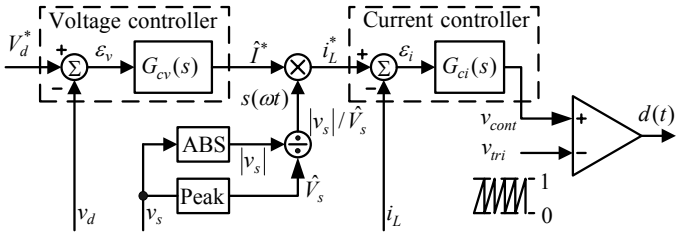

Fig. 2. Conventional multi-loop control for boost-type SMRs.

III. Proposed Duty Phase Control

The configuration of the proposed DPC is plotted in Fig. 3 where only one voltage controller is used. The DPC technique can be regarded as a single-loop control. Like the conventional configuration in Fig. 2, the duty signal $d(t)$ is also generated by comparing the carrier signal v_{tri} and the control signal v_{cont}. Noted that the carrier signal v_{tri} is at (+) terminal in Fig. 3, but at (-) terminal in Fig. 2. Besides, the control signal v_{cont} is not the current controller output as in Fig. 2 but is the pre-defined duty which is the product of the gain $\hat{V}_s / V_d$ and the shifting rectified signal $s(\omega t - \theta)$ from the signal $s(\omega t)$ in Fig. 3. The control signal v_{cont} and the average duty signal $\bar{d}(t)$ can be expressed in the following two equations:

$$v_{cont}(t) = \frac{\hat{V}_s}{V_d} \left| \sin(\omega t - \theta) \right| \tag{7}$$

$$\bar{d}(t) = 1 - \frac{\hat{V}_s}{V_d} \left| \sin(\omega t - \theta) \right| \tag{8}$$

where the maximum duty is 100% and the minimum average duty is dependent on the input voltage amplitude $\hat{V}_s$ and the average output voltage V_d. From (8), we can find that the duty pattern is in fact pre-defined.

To simply the following analysis, the main circuit topology in Fig. 1 and the proposed DPC in Fig. 3 can be combined and redrawn in Fig. 4 where the diode rectifier is removed. Thus, the input voltage of the boost-type DC/DC converter is

represented as an ideal rectified sinusoidal voltage $\hat{V}_s|\sin(\omega t)|$. In the following derivations, we will show that the inductor current will become rectified sinusoidal waveform by the pre-defined patterns. Therefore, the SMR's current shaping function is achieved.

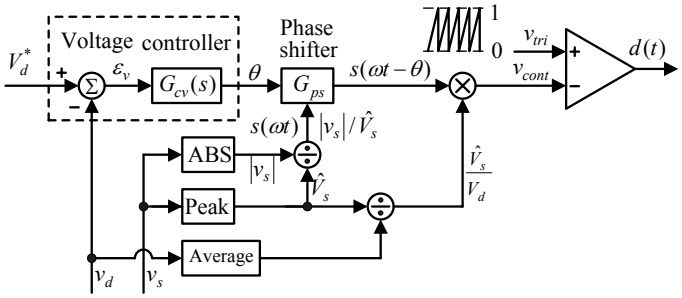

Fig. 3. Proposed DPC for boost-type SMRs.

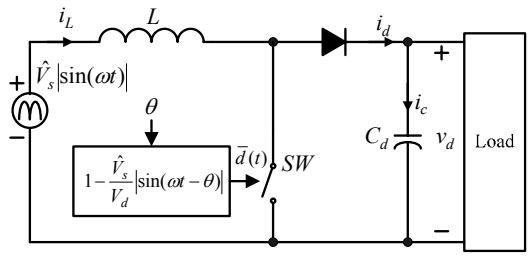

Fig. 4. Boost-type PFC SMR with DPC.

From Fig. 4, the KVL and KCL equations can be written as the following equations according to the conduction states pf power switch *SW*.

$$L\frac{di_L(t)}{dt}=\hat{V}_s|\sin(\omega t)| \quad \text{when } SW \text{ is turning on} \tag{9}$$

$$L\frac{di_L(t)}{dt}=\hat{V}_s|\sin(\omega t)|-V_d \quad \text{when } SW \text{ is turning off} \tag{10}$$

Based on the time-averaging approach, the above two equations can be combined to become the following equation (11) through multiplying them by turning-on time $\bar{d}(t)T_s$ and turning-off time $(1-\bar{d}(t))T_s$, respectively.

$$L\frac{d\,i_L(t)}{dt}=\hat{V}_s|\sin(\omega t)|-(1-\bar{d}(t))V_d \tag{11}$$

Therefore, by substituting the duty signal $\bar{d}(t)$ into the above equation and arranging the terms, we can obtain the following time-differential equations for inductor current.

$$\frac{d\,i_L(t)}{dt}=\frac{\hat{V}_s|\sin(\omega t)|}{L}-\frac{\hat{V}_s|\sin(\omega t-\theta)|}{L} \tag{12}$$

The right term $\sin(\omega t-\theta)$ can be extracted by applying the commonly used function $\sin(A-B)=\sin A\cos B-\sin B\cos A$. If the duty phase signal θ in radians is small and near to zero ($\theta\approx 0$), we can substitute $\sin\theta\approx\theta$ and $\cos\theta\approx 1$ and the above equation can be rewritten as:

$$\frac{d\,i_L(t)}{dt}\approx\frac{\hat{V}_s|\sin(\omega t)|}{L}-\frac{\hat{V}_s|\sin(\omega t)-\theta\cos(\omega t)|}{L} \tag{13}$$

Since the inductor current is periodic with double line frequency, the current differential equation during the first cycle ($0\le\omega t<\pi$) can be approximately obtained by removing the absolute operators in (13) and canceling the same terms $\sin(\omega t)$.

$$\frac{d\,i_L(t)}{dt}\approx\frac{\hat{V}_s\theta\cos(\omega t)}{L},\quad 0\le\omega t<\pi \tag{14}$$

Then, by integrating (14), we can obtain the first-cycle current as

$$i_L(t)\approx\frac{\hat{V}_s\theta}{\omega L}\sin(\omega t),\quad 0\le\omega t<\pi \tag{15}$$

where the current magnitude is dependent on the duty phase θ. Because of the periodic current in inductor, we can write the complete inductor current $i_L(t)$ in terms of the first-cycle current in (15).

$$i_L(t)\approx\frac{\hat{V}_s\theta}{\omega L}|\sin(\omega t)|=\hat{I}_s|\sin(\omega t)| \tag{16}$$

Noted that the inductor current waveform becomes the rectified sinusoidal waveform and the current amplitude $\hat{I}_s$ is nearly proportional to the duty phase θ. From the original circuit topology including diode bridge rectifier as shown in Fig. 1, the relation between the input current $i_s(t)$ and inductor current $i_L(t)$ can be express as

$$i_s(t)=\begin{cases} i_L(t) & when\ v_s=\hat{V}_s\sin\omega t\ge 0\\ -i_L(t) & when\ v_s=\hat{V}_s\sin\omega t<0\end{cases} \tag{17}$$

However, equation (17) can be simplified to the sinusoidal waveform $\hat{I}_s\sin\omega t$ in phase with the input voltage $\hat{V}_s\sin\omega t$. It implies that by using the proposed pre-defined duty pattern, the aligning sinusoidal current waveform can be obtained without current feedback.

Besides, because the input current amplitude $\hat{I}_s$ can be controlled by its dependency on the duty phase θ, we are able to regulate the input and output power with unity power factor by tuning the duty phase θ. That is, we can include a voltage controller in DPC to obtain suitable duty phase θ to meet the requirement of current waveform shaping and output voltage regulation.

In addition, the output voltage ripple in (6) can be rewritten by replacing the term $\hat{I}_s$ with (16):

$$v_{d,ac}(t)\approx-\frac{\hat{V}_s^2\theta}{4\omega^2LC_dV_d}\sin(2\omega t) \tag{18}$$

IV. Simulated Results

In this section, we begin with a series of computer simulations to demonstrate the proposed DPC. Some nominal values and circuit elements are listed in Table I. It should be noted that no design optimization has been done in order to select the values in Table I. The simple plus-integral (PI) controller is used in the voltage loop of the developed DPC to adjust the duty phase.

Table I
Simulated circuit parameters

Input line voltage (peak)	$\hat{V}_s = 170V\ (120V_{rms})$
Input line frequency	$f = 50Hz$
Smoothing capacitance	$C_d = 560\mu F$
Smoothing inductance	$L = 4.65mH$
Equivalent load resistance	$R_{load} = 200\Omega(\|\|1600\Omega)$ $= 200\Omega$ or 177.78Ω
Carrier frequency	$f_{tri} = 25kHz$

The simulated waveforms for the condition V_d^*=300V and $R_{load} = 200\Omega$ are plotted in Fig. 5 where the average duty signal $\overline{d}(t)$ and the reference signal (i.e. zero duty phase $\theta = 0$) are the solid line and the dashed line, respectively, in the upper plots. From the simulated data, the duty phase is about 0.014π rads to obtain the desired output voltage v_d shown in the bottom plot. It implies tuning the duty phase is able to regulate the output voltage.

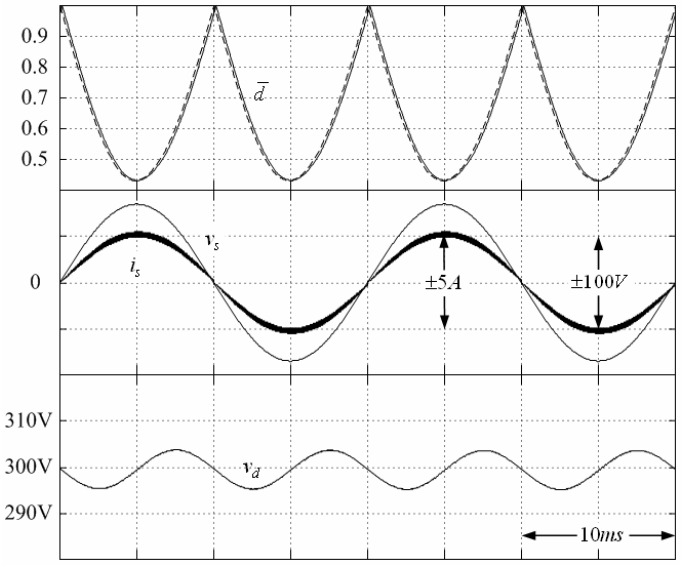

Fig. 5. Simulated waveforms for ideal circuit elements.
Top: average duty signal. Middle: input current and voltage.
Bottom: output voltage.

From the middle plot, we can find that input current is sinusoidal waveform in phase with the input voltage and therefore, not only the output voltage regulation but the input current shaping can be achieved by the single loop tuning the single duty phase. Furthermore, from the key derived equation in (16) and the parameters in Table I, we can calculate and find that the input current peak is about 5.12A. From observing the input current amplitude 5.1A in the middle plot, the key equation in (16) has been demonstrated.

However, the above simulated waveforms in Fig. 5 are based on the strong assumption of ideal circuit elements. In the following simulations, all the equivalent resistors of inductor and bulk capacitor and the voltage drops of diodes and switch are included in the simulation program to evaluate the nonideal effect on the performance of the proposed DPC.

The simulated waveforms for the same condition V_d^*=300V and $R_{load} = 200\Omega$ are plotted in Fig. 6. The average duty signal $\overline{d}(t)$ (solid line) and duty reference signal (dashed line) are plotted together in the upper plots for the sake of comparison. From the simulated data, the duty phase θ now is increasing to about 0.024π rads to obtain the desired output voltage found in the bottom plot. Thus, the actual circuit elements have no effect on the output voltage regulation in the proposed DPC.

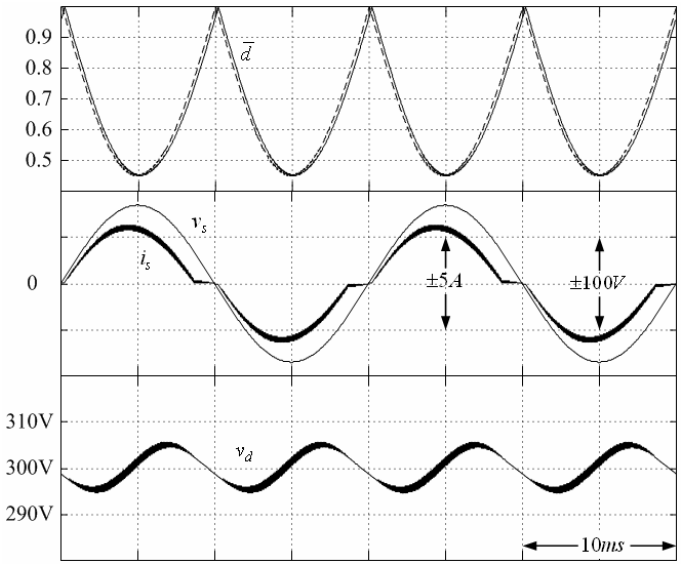

Fig. 6. Simulated waveforms for ideal circuit elements.
Top: average duty signal. Middle: input current and voltage.
Bottom: output voltage.

However, from the middle plot in Fig. 6, we can find that the ideal sinusoidal current waveform in Fig. 5 has been distorted and replaced with the incomplete sinusoidal waveform where the near-zero portion has been cut. Since the current waveform is far from the sinusoidal one, it is reasonable that the duty phase θ increases from 0.014π rads to 0.024π rads in order to provide larger current magnitude and thus, to obtain the desired output voltage. Fortunately, from the following experimental results, the harmonic currents of such distorted current waveform are still lower than the limits of standard IEC 61000-3-2. It implies the developed DPC technique complies with IEC 61000-3-2.

Then, we increase the load condition R_{load} =177Ω with the same voltage command V_d^* =300V and illustrate the experimental waveform in Fig. 7. In order to yield suitable

current amplitude to meet the new load condition, the duty phase is automatically tuned to about $\theta \approx 0.028\pi$ rads through the voltage loop.

From (8), all the duty patterns in Fig. 5 through Fig.7 are the same because of the same input and output voltage level. The only differences between them are their phase which is the main originality of the proposed DPC. In addition, although the current waveforms are not sinusoidal ones, the proposed DPC still possess useful input and output performances.

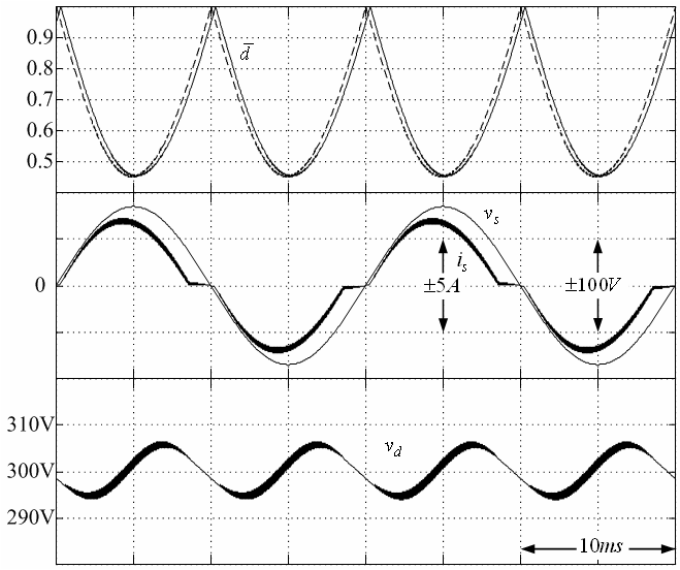

Fig. 7. Simulated waveforms for ideal circuit elements. Top: average duty signal. Middle: input current and voltage. Bottom: output voltage.

IV. Realization

The proposed DPC has been digitally implemented in a DSP-based system using TMS320F240 where a simple and popular PI-type voltage loop is used in order to focus on the performance of tuning duty phase. Only input voltage and output voltages are sensed where the former provides the phase information of input voltage and the latter helps to regulate the output voltage. It is noted that the digital resolution of duty phase is the main challenge in the implementation of the proposed DPC. Too smaller resolution will result in the instable operation of SMRs in shaping current waveform. In my experiment, the phase resolution is set to 12500 per π rads. All the circuit parameters in the experimental system had been listed in Table. I.

V. Experimental Reslts

Fig. 8 shows the measured waveforms for the condition $V^* = 300V$ and $P_s \approx 520W$. The top plot shows the output voltage waveform varying around the desired voltage level. The duty phase signal in the middle plot is almost fixed to 0.028π rads in order to stably yield the input current as shown in the bottom plot. From the bottom plots of input current and voltage, we can find that the actual current waveform is very close to the simulated one in Fig. 7 and the measured power factor now is 0.944. Obviously, input power quality has been improved and the proposed DPC has been demonstrated.

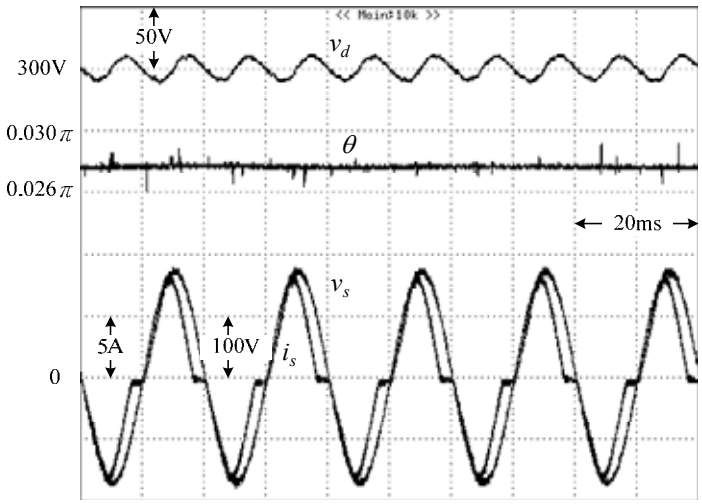

Fig. 8. Measured waveforms at $P_s = 520W$. Top: output voltage. Middle: duty phase. Bottom: input current and voltage.

In Fig. 9, the average duty phase signal $\bar{d}(t)$ is shown and the reference signal is also plotted for comparison. We can find that the little phase difference between the top plots contributes to draw the distorted current waveform similar to the waveform shown in Fig. 7.

Fig. 10 shows the measured waveforms at $V^* = 300V$ and input power $P_s = 456W$. In order to draw smaller current amplitude for smaller input power, the duty phase signal in the middle plot is automatically adjusted from about 0.028π rads to 0.024π rads by the voltage loop. It also implies that the proposed DPC is able to vary the output voltage simply by varying the phase of the per-defined duty pattern.

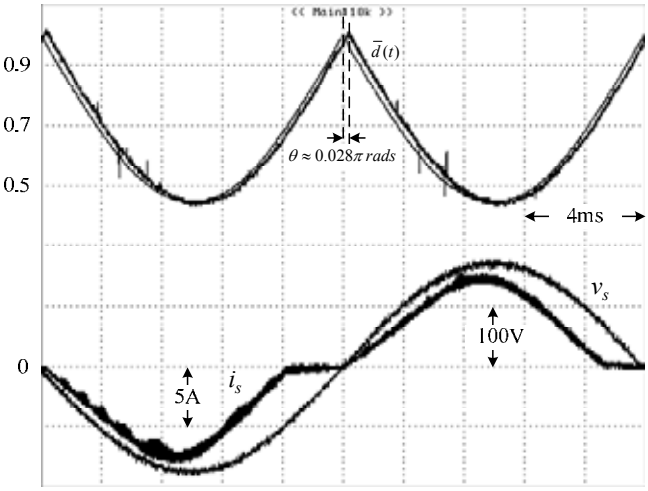

Fig. 9. Measured waveforms at $P_s = 520W$. Top: average duty signal. Bottom: input current and voltage.

In addition, by using digital power meter YOGOGAWA WT210, the measured power factor, the total current harmonic distortion and the harmonic currents are listed in Table II where the limits IEC-61000-3-2 are also tabulated for the sake of comparison. The total harmonic distortion is about 23.22% and 24.57% in both cases. Fig. 11 plots the harmonic spectra of input current for the measurement in Fig. 8 and Fig. 10. From Fig. 11 and Table II, we can find that the developed control technique generates input current harmonics well below the limits of IEC-61000-3-2 and the current control loop for current tracking has been eluded. This illustrates the advantages of the developed control technique – the proposed DPC is very simple as it avoids inner current loop, and the technique is robust as it has an inherent ability to shape current waveform.

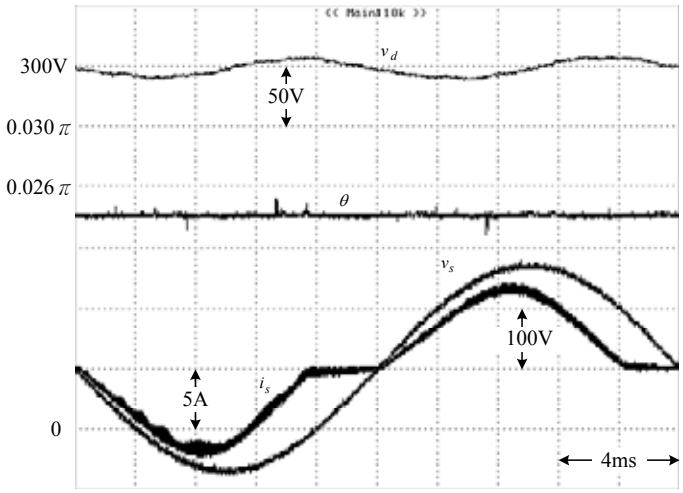

Fig. 10. Measured waveforms at $P_s = 456W$. Top: output voltage. Middle: duty phase. Bottom: input current and voltage.

Table II
Harmonic currents

	IEC-61000-2-3	$P_s = 520W$ PF=0.944 THD=24.57%	$P_s = 456W$ PF=0.953 THD=23.2%
n=3	2.30 A_{rms}	0.9918 A_{rms}	0.8371 A_{rms}
n=5	1.14 A_{rms}	0.1642 A_{rms}	0.1624 A_{rms}
n=7	0.77 A_{rms}	0.1043 A_{rms}	0.0982 A_{rms}
n=9	0.40 A_{rms}	0.0364 A_{rms}	0.0309 A_{rms}
n=11	0.33 A_{rms}	0.1118 A_{rms}	0.1026 A_{rms}
n=13	0.21 A_{rms}	0.0930 A_{rms}	0.0850 A_{rms}
n=15	0.15 A_{rms}	0.0140 A_{rms}	0.0194 A_{rms}
n=17	0.13 A_{rms}	0.0175 A_{rms}	0.0166 A_{rms}
n=19	0.12 A_{rms}	0.0094 A_{rms}	0.0136 A_{rms}

V. CONCLUSIONS

A new DPC has been developed to the boost-type SMRs, which just adjusts the phase of pre-defined duty pattern. The control technique is single-loop and no current control loop is included. It means that the system cost could be notably decreased for the needless current sampling and/or ADC. Therefore, the DPC is very simple for analog and digital implementations.

The new DPC technique described and considered in this paper is a generation of popular multi-loop control technique, which can be used directly in many other applications. Simulation and experimental results verify the functionality of the developed DPC technique, where the input harmonic currents compile with IEC 61000-3-2. The developed control can be advanced by considering the nonideal effect on the current waveform in order to provide an even higher power-factor and total current harmonic distortion.

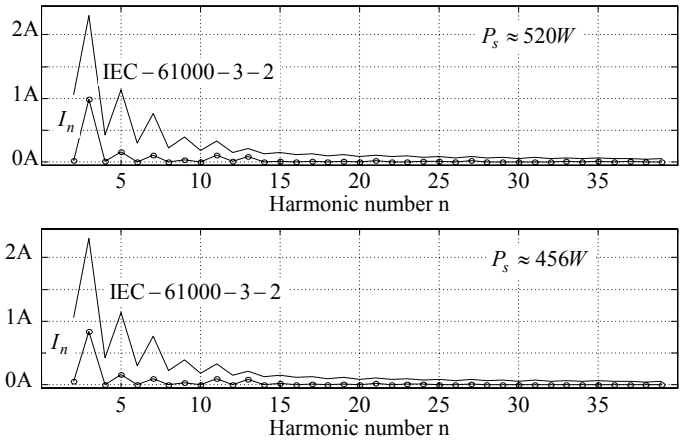

Fig. 11. Harmonic spectra of the input current and the IEC-61000-3-2 limits. Top: the harmonic current for the measurement in Fig. 8. Bottom: the harmonic current for the measurement in Fig. 10.

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REFERENCES

[1] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, 'Single phase Power Factor Correction: A Survey,' *IEEE Trans. on Power Electronics*, vol. 18, no. 3, pp. 749-754, May 2003.

[2] J. B. Williams, "Design of feedback loop in unity power factor AC to DC converter," in *Proc. PESC'89*, 1989, pp. 959-967.

[3] H. C. Chen, S. H. Li, and C. M. Liaw, "Switch-Mode Rectifier With Digital Robust Ripple Compensation and Current Waveform Controls", *IEEE Trans. on Power Electronics*, vol. 19, no. 2, pp. 560-566, Mar. 2004.

[4] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche, and J. A. Melkbeek, 'Duty-Ratio Feedforward for Digitally Controlled Boost PFC Converters,' *IEEE Trans. on Industrial Electronics*, vol. 52, no. 1, pp. 108-115, Feb. 2005.

[5] M. Chen, and J. Sun, 'Feedforward Current Control of Boost Single-Phase PFC Converters,' *IEEE Trans. on Power Electronics*, vol. 21, no. 2, pp. 338-345, Mar. 2006.

[6] E. Fiqueres, J. M. Benavent, G. Garcera and M. Pascual, "Robust Control of Power-Factor-Correction Rectifiers with Fast Dynamic Response," *IEEE Trans. on Industrial Electronics*, vol. 52, no. 1, pp. 66-76, Feb. 2005.

[7] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive Digital Current Programmed Control," *IEEE Trans. on Power Electronics*, vol. 18, no. 1, pp. 411-419, Jan. 2003.

[8] W. Zhang, G. Feng, Y. F. Liu, and B. Wu, 'A digital Power Factor Correction (PFC) Control Strategy Optimized for DSP,' *IEEE Trans. on Power Electronics*, vol. 19, no. 6, pp. 1474-1485, Nov. 2004.